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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/539,458	03/30/2000	Mark S. Chang	1346P/DA01028	8108

7590 05/22/2002

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EXAMINER

PHAM, HOAI V

ART UNIT	PAPER NUMBER
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2814

DATE MAILED: 05/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/539,458

Applicant(s)

CHANG ET AL.

Examiner

Hoai V Pham

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 23 January 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) 8-16 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                             | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____  |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)         | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____                                    |

**DETAILED ACTION**

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (hereinafter AAPA) in view of Paterson et al. [U.S. Pat. 5,065,220].

Applicant Admitted Prior Art discloses a flash memory device comprising:

a plurality of gate stacks including a plurality of floating gates (62) and a plurality of control gates (66) disposed on a semiconductor substrate;

at least one component including a polysilicon layer (76) having a top surface;

an insulating layer (80) covering the plurality of gate stacks, the at least one component, the insulating layer having a plurality of contact holes (82, 84, 86) and a conductor filling the plurality of contact holes, wherein the silicide layer not resides between the plurality of floating gate and the plurality of control gates in the plurality of gate stacks.

Applicant Admitted Prior Art does not teach a silicide on the top surface of the polysilicon layer of the at least one component and the insulating layer etching step using the silicide as an etch stop layer to ensure that the insulating etching step does not etch through the polysilicon layer. However, Paterson et al. shows that it is conventional in the art to have a device with a silicide (14) on top surface of the polysilicon layer (12) wherein the contact hole (26) being formed through the insulating layer (16) and stopped at the silicide film (14) to improve stability of the underlying polysilicon (see figures 1-2, cols. 2-5). Therefore, it would have been obvious to the skilled in the art to use silicide on the top surface of the polysilicon layer in the Applicant Admitted Prior Art device to provide a better device with an improved stability of the polysilicon and a further reduced resistance of the polysilicon.

With respect to claim 2, Paterson et al. shows that the silicide further includes a titanium silicide (see col. 3, lines 45-46).

With respect to claim 3, Paterson et al. does not particularly mention that the silicide further includes a cobalt silicide. However, Paterson et al. shows that any refractory metal can be used for silicide (see col. 3, lines 45+). Since cobalt is well

known refractory metal, it would have been obvious to use cobalt silicide in the device of Applicant Admitted Prior Art in view of Paterson et al.

With respect to claim 6, Applicant Admitted Prior Art discloses that the plurality of gate stacks further include a plurality of spacers (74) (see figure 2).

With respect to claim 7, Applicant Admitted Prior Art discloses that at least one field oxide region (54), the at least one component being located on the at least one field oxide region (see figure 2).

With respect to claims 4, 5 and 6, Paterson et al. shows that oxide-nitride-oxide layers (20, 22) on the polysilicon (12) (see col. 4, lines 30-38).

Note that process limitation in claims 1, 5 and 6 (oxide-nitride-oxide layer is removed prior to formation of the silicide; removed during a second polysilicon layer etching step or removed after formation of the plurality of spacers.) do not carry weight in a claim drawn to structure. *In re Thorpe*, 227 USPQ 964 (Fed. Cir. 1985). In addition, a "product by process" limitation is directed to the product per se, no matter how actually made, in *re Hirao*, 190 USPQ 15 and 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90; and *In re Marosi et al.*, 218 USPQ 289; all of which made clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product by a new method is not patentable as a product, whether claimed in "product by process" claims or not.

***Response to Arguments***

4. Applicant's arguments filed January 23, 2002 have been fully considered but they are not persuasive.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the silicide on top surface of the polysilicon layer is well known in the art to reduce resistance of the polysilicon. However, Paterson et al. shows that it is conventional in the art to have a device with a silicide (14) on top surface of the polysilicon layer (12) wherein the contact hole (26) being formed through the insulating layer (16) and stopped at the silicide film (14) to improve stability of the underlying polysilicon (see figures 1-2, cols. 2-5). Therefore, it would have been obvious to the skilled in the art to use silicide on the top surface of the polysilicon layer in the Applicant Admitted Prior Art device to provide a better device with an improved stability of the polysilicon and a further reduced resistance of the polysilicon.

In response to applicant's argument that "Paterson is concerned with the formation of capacitor in a device". This argument is not persuasive since the invention

relates to the silicide on the polysilicon to ensure that the insulating etching step does not etch through the polysilicon layer and has nothing to do with what type of the device.

In response to applicant's argument that "Paterson is added to those of the AAPA, the combination would still fail to teach or suggest that the silicide layer on the first component that resides on the first polysilicon layer does not reside between the plurality of floating gates and the plurality of control gates in the plurality of gate stacks". This argument is not persuasive since in the AAPA device, the silicide layer does not reside between the plurality of floating gates and the plurality of control gates in the plurality of gate stacks. The AAPA does not teach a silicide on the top surface of the polysilicon layer of the at least one component. However, Paterson et al. shows that it is conventional in the art to have a device with a silicide (14) on top surface of the polysilicon layer (12) as mention above. Therefore the rejection is proper.

### ***Conclusion***

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).
6. A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai V Pham whose telephone number is 703-308-6173. The examiner can normally be reached on 6:30A.M. - 6:00P.M..

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

9. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

HP  
Hoai Pham  
May 17, 2002

  
OLIK CHAUDHURI  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800